IN THE SPECIFICATION

Please replace the following paragraphs:

Page 3, paragraph [0008].

**[0008]** In another embodiment, an information handling system (IHS) is disclosed which includes a processor and a memory coupled to the processor. ~~The IHS also includes a memory coupled to the processor.~~ The IHS further includes glue logic, coupled to the processor, for enabling devices to be coupled to the processor. The IHS still further includes a receiver, coupled to the glue logic, for receiving commands and a remote control for sending commands to the receiver. The method also includes nonvolatile storage, coupled to the glue logic, including control software for causing the IHS to enter a reduced power mode in response to the receiver receiving a command from the remote control and, upon loss of power by the IHS and return of power to the IHS, instructing that power be supplied to a sufficient portion of the IHS to enable the IHS to respond to commands from the remote control.

Page 4, paragraph [0010].

**[0010]** FIG. 1 is a block diagram illustrating an embodiment of the disclosed information handling system (IHS).

Page 4, paragraph [0011].

**[0011]** FIG. 2 is a representation illustrating an embodiment of the power planes of the disclosed IHS.

Page 4, paragraph [0012].

**[0012]** FIG. 3 is a diagram illustrating an embodiment of an OR gate used to generate a power on/wake signal for the IHS.

Page 7, paragraph [0019].

**[0019]** IHS 100 is designed to have BIOS power behavior which solves the wake up problem described earlier where the remote user presses the power button on the remote control when power is restored to the system after being lost while the IHS is in a reduced power or suspend mode. The IHS will now again commence operation after restoration of power. However, instead of fully booting the operating system, the IHS enters a minimal power on self test (POST) mode. In this minimal POST mode, a minimal number of devices are activated, namely the devices needed to load a BIOS peripheral bus driver, for example, the USB driver in this case. Once the minimal POST mode is entered, the IHS waits for the user to press IR remote power button 195 or main power button switch 165. To the user, it appears that IHS 100 is off ~~since~~ because display 120, media drives 180 and other devices are not operating.

Page 8, paragraph [0021].

**[0021]** FIG. 2 is a diagram representing the power planes of IHS 100. IHS 100 includes an I/O power plane 201, a RAM power plane 202, a core power plane 203, a PCI power plane 204, a USB power plane 205 and real time clock (RTC) power plane 208. RTC power plane 208 is connected to an RTC battery 209 such that RTC power plane 208 always has power even when IHS 100 is turned off or is otherwise without power. Power planes 201, 202, 203, 204 and 205 are coupled to

respective voltages VCC through respective switching FETs 211, 212, 213, 214 and 215. Each of switching FETs 211, 212, 213, 214 and 215 is supplied with a respective ENABLE signal so that power planes 201 – 205 can be individually turned on and off. In other words, one switching plane, such as USB power plane 205 for example, can be turned on without turning on the other power planes. The voltages VCC supplied to the respective power plans 201 – 205 can be different voltages.